

PILC



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Hamburg, 20.09.2023

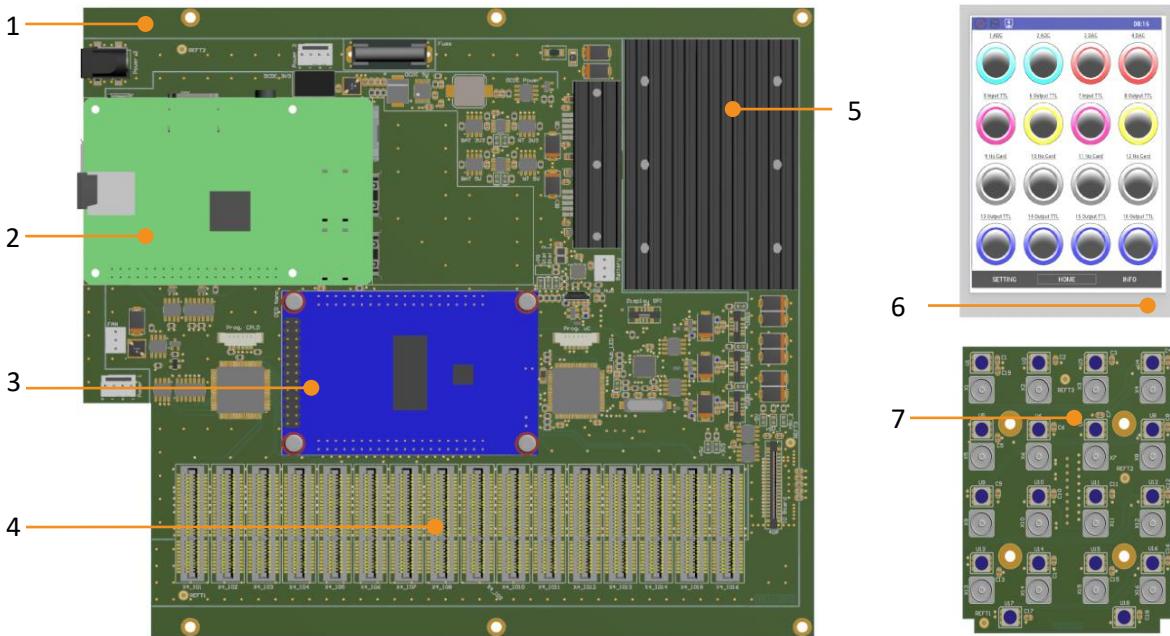
PiLC – History

- First ideas for the PiLC 2012:
 - *To have a flexible and easily customizable module for fast signal processing.*
 - *Independently from third**.
 - *Use existing infrastructure.*
 - *Read and write data over Tango.*
 - *Update firmware over Tango.*
 - *Possible to use different input/output signals (digital and analog).*
 - *Touchdisplay to present the data / states direct on site.*
 - *Low cost*
- First prototype build in 2013



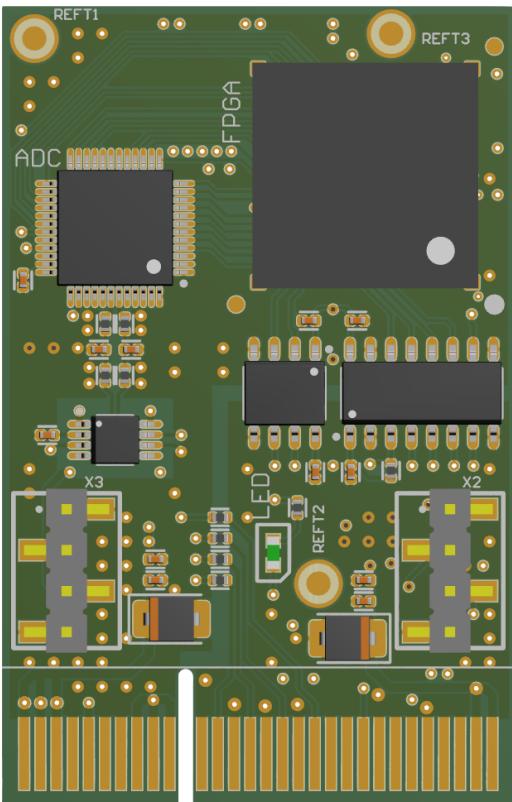
PiLC – Components

1. Mainboard
2. Embedded Computer (Raspberry Pi)
3. FPGA
4. 16 slots for I/O cards
5. Power supply unit
6. Touchscreen
7. I/O board with 16 coaxial LEMO connectors and 18 RBG LEDs

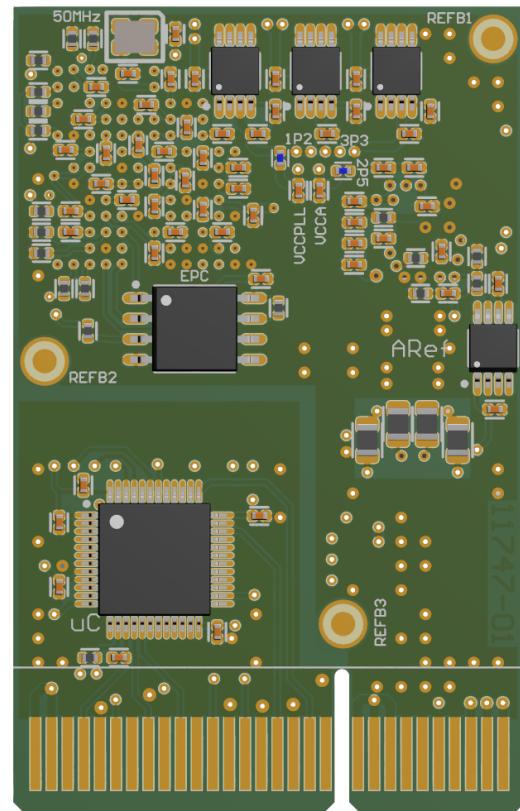


PiLC – IO Cards

- IO NIM/TTL 50Ω
- ADC: 0-10V, 16Bit, 1MS/s
- DAC: 0-10V, 16Bit, 1MS/s
- PT resistor: PT10, PT100, PT500, PT1000
- Differential ADC: -10V - 10V, 18Bit, 2MS/s
- Thermocouple: Types K,R,T,S



Diff. ADC Top



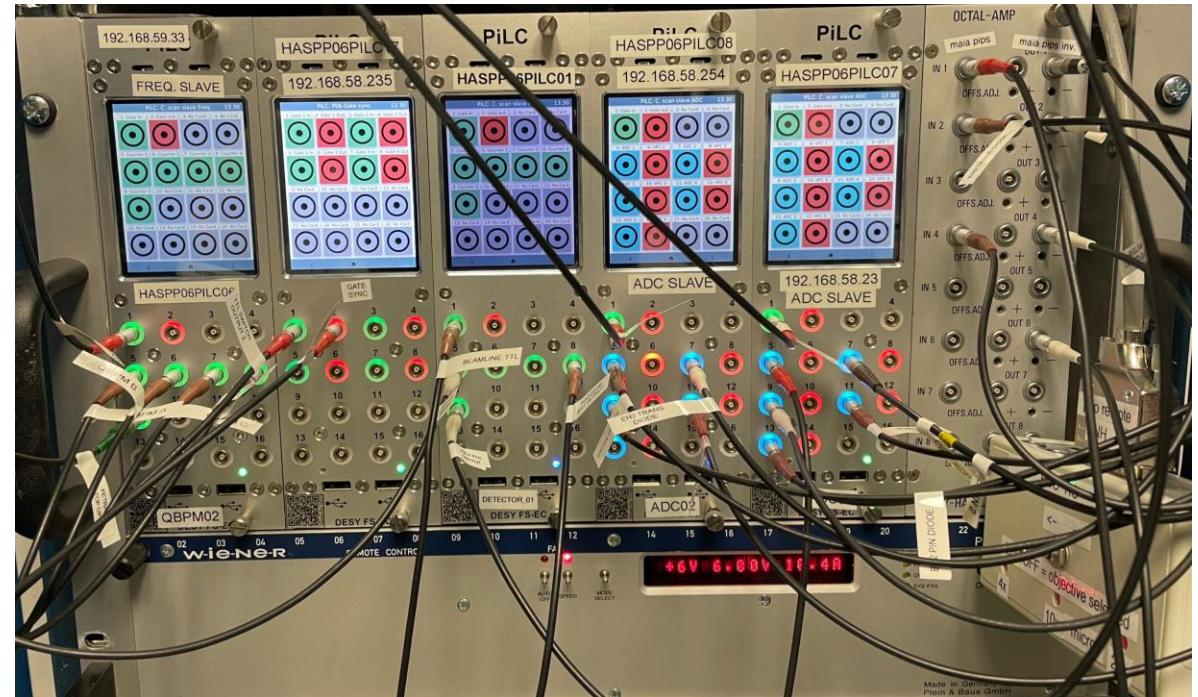
Diff. ADC Bot

PiLC – Distribution 2023

- Over 100 PiLC operational @ PETRA III and FLASH
 - Sold one to the Max-Born-Institute
 - Over 30 different configuration and FPGA Firmware

For example:

 - Continuous scans.
 - Shutter controller.
 - Volt to frequency converter.
 - PID heater controller.
 - Array based trigger generator.
 - Gate generator based on a rotation stage index signal.



PiLC @ P06

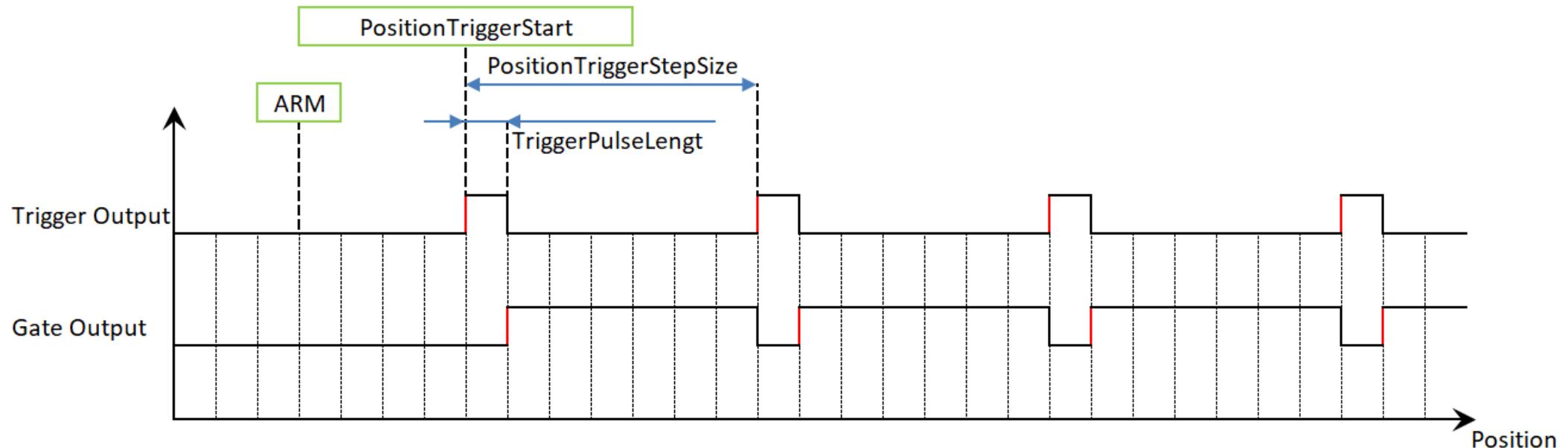
PiLC – Firmware – Continuous scans

- Generates trigger or gate signals depending on encoder position or a time base.
- Different scan modes.
- Write data to a nexus file.
- Maximum 2kHz repetition rate.
- Main PiLC stores Up to 5 encoders & 1 counter.
- To store additional / different signals like ADC values, it is possible to daisy chain PiLCs.
- Requires an encoder splitter

PiLC – Firmware – Continuous scans

- Start and steps encoder based

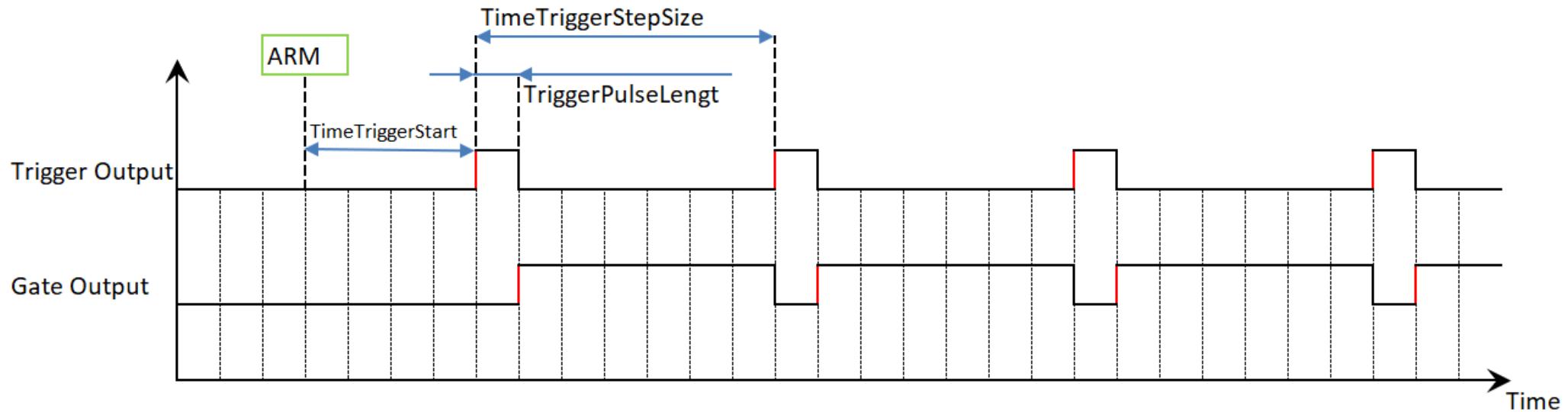
Example: Trigger generation starts at encoder pos. 100 and every 10 encoder steps a trigger is generated



PiLC – Firmware – Continuous scans

- Start and steps time based

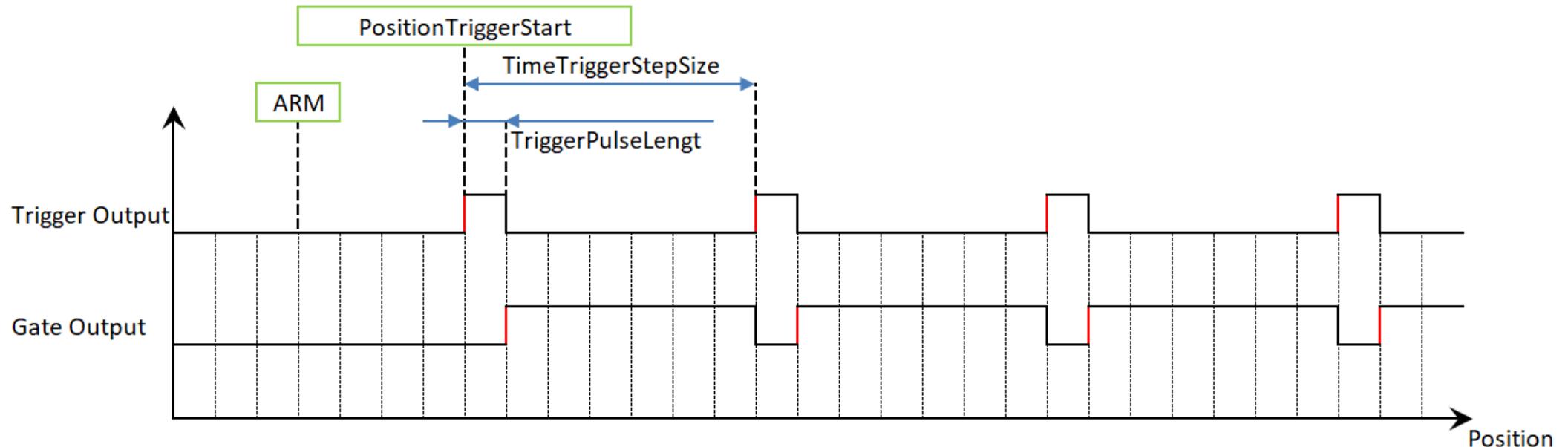
Example: Trigger generation starts at encoder pos. 100 and every 10 encoder steps a trigger is generated



PiLC – Firmware – Continuous scans

- Start: Encoder Position; Steps: Time based

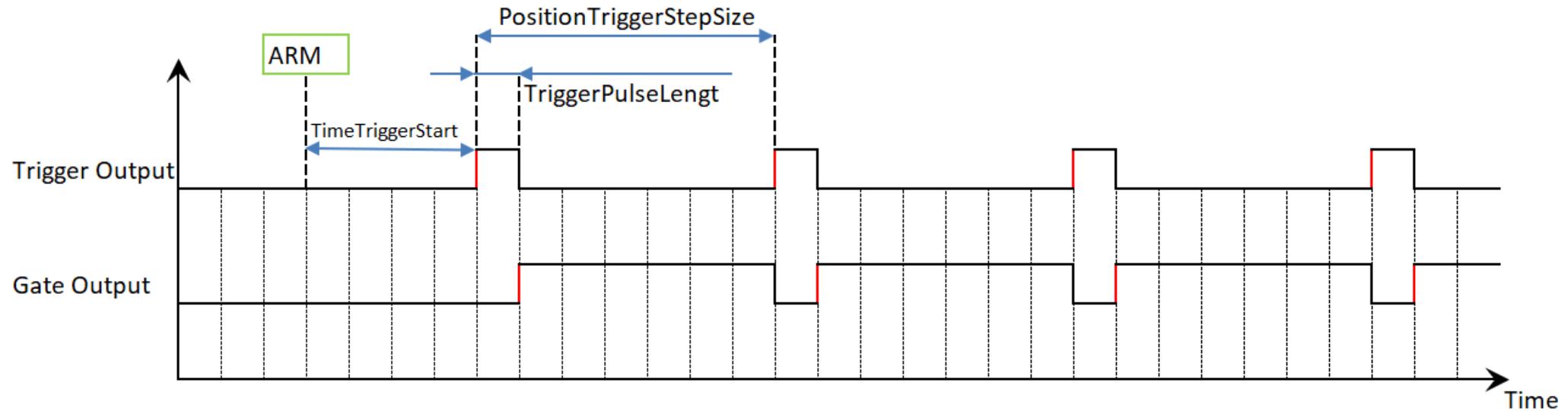
Example: Trigger generation starts at encoder pos. 100 and every 10ms a trigger is generated



PiLC – Firmware – Continuous scans

- Start: Time based; Steps: Encoder Position

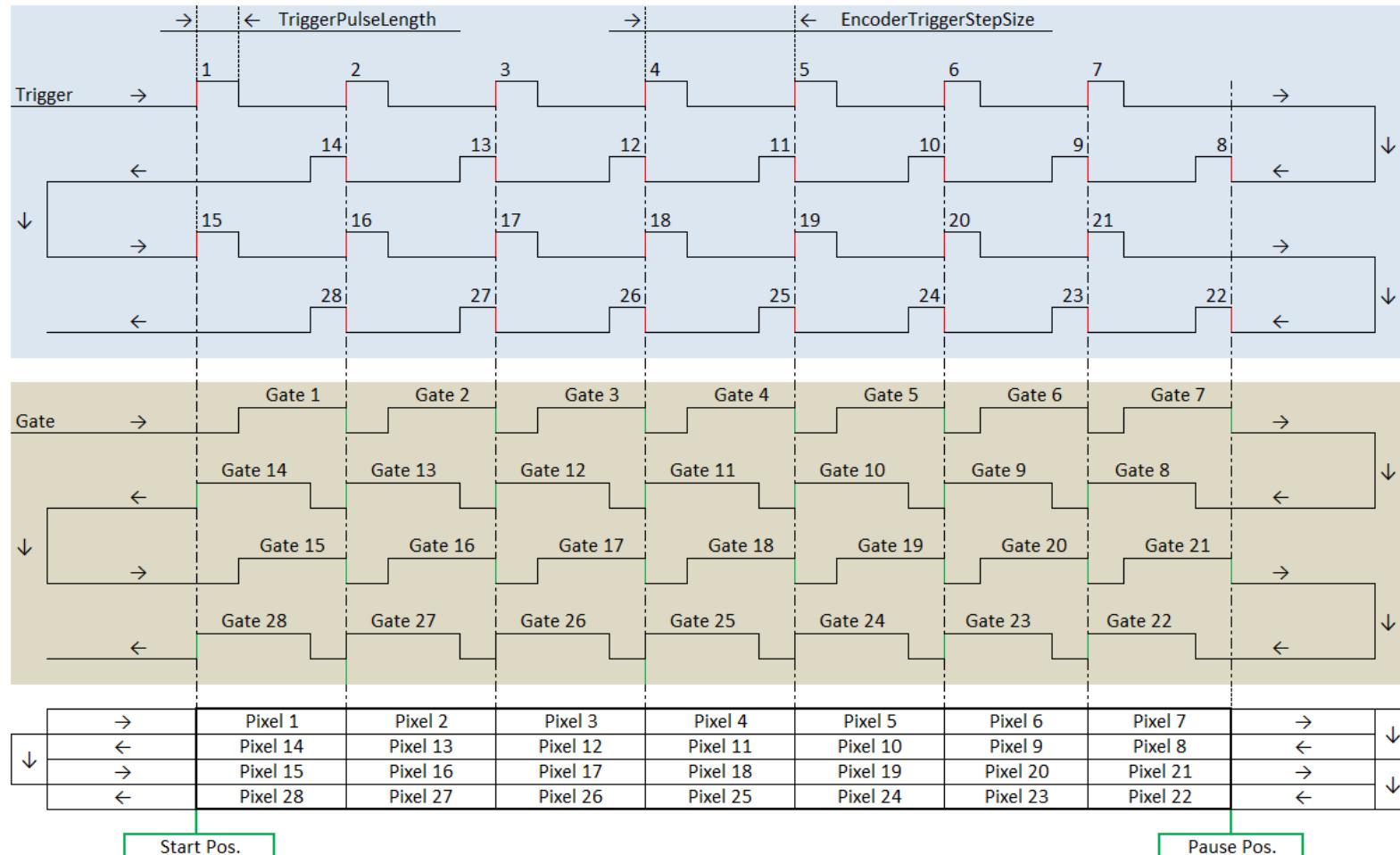
Example: Trigger generation starts at encoder pos. 100 and every 10ms a trigger is generated



PiLC – Firmware – Continuous scans

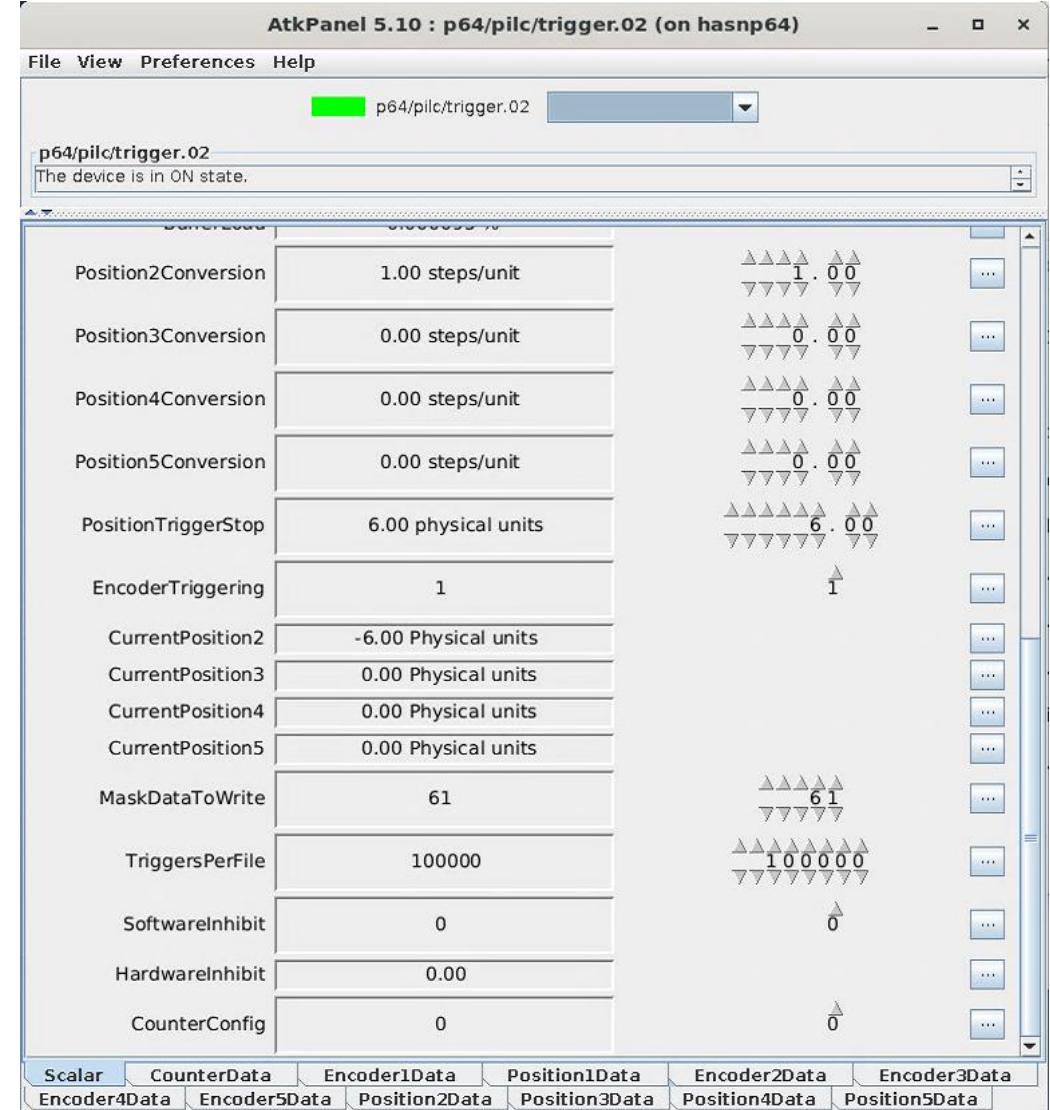
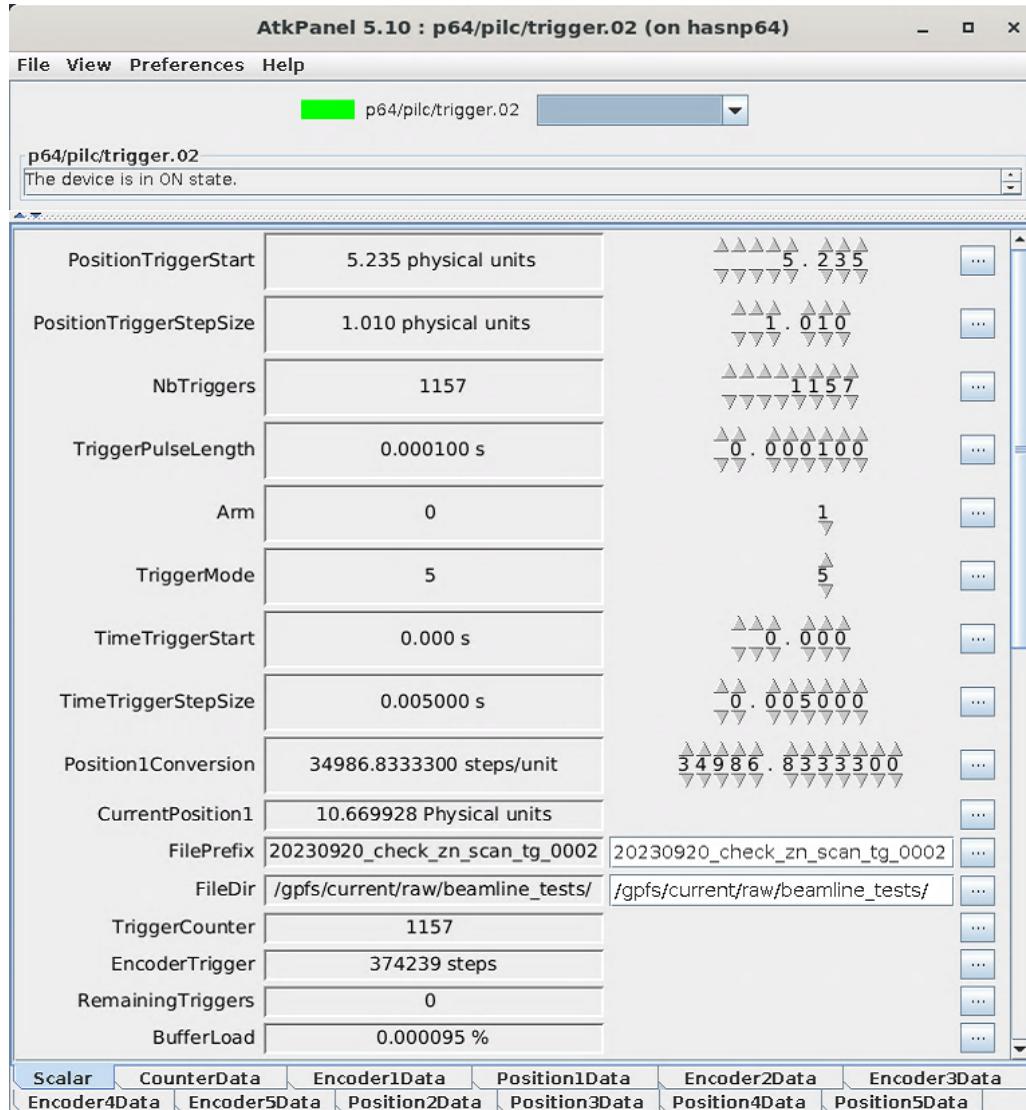
- Start: Encoder Position; Steps: Encoder Position; Pause: Encoder Position

Example: Trigger generation starts at encoder pos. 100 and every 10 encoder steps a trigger is generated. The Trigger generation pause, when encoder pos. is 1000



PiLC – Firmware – Continuous scans

- Tango Server



PiLC – Status Website

Tango Host Auswahl: haspp01eh2:10000/p01/pilc... Filter: haspp01eh2

Manuelle Eingabe:

● PiLC Status: haspp01eh2:10000/p01/pilc/exp.01 Online

FPGA IO Cards IO Board Display Mainboard

FPGA Infos					
ID	Hardware Version	Software Version	Projekt Nummer	Projekt Name	Projekt Version
0xec	11	11	10	Continuous scan	12

IO Uebersicht							
Nummer	Richtung	Name	Status	In Register	In Bez.	Out Register	Out Bez.
1	Input	Enc 1 A	0	0	Control	7574371	Position 1
2	Input	Enc 1 B	0	22302359	Start value	0	Position 2
3	Input	Trig./Gate	0	10200	Step value	0	Position 3
4	Input	Counter In	0	100000	Trigger end value	0	Position 4
5	Input	Enc 2 A	0	11176005	Enc 1 load	0	Position 5
6	Input	Enc 2 B	0	10000	Trigger decay	0	Trigger counter
7	Input	Enc 3 A	0	0	Enc 2 load	0	Save counter
8	Input	Enc 3 B	0	0	Enc 3 load	112	not used
9	Input	Enc 4 A	0	0	Enc 4 load	7609609	not used
10	Input	Enc 4 B				88523	not used
11	Input	Enc 5 A				88808	not used
12	Input	Enc 5 B				1	not used
13	Output	Trigger Out				0	not used
14	Output	Gate Out				0	Counter Out
15	Input	Inhibit				0	HW Inhibit State
16	Output	not used				0	not used

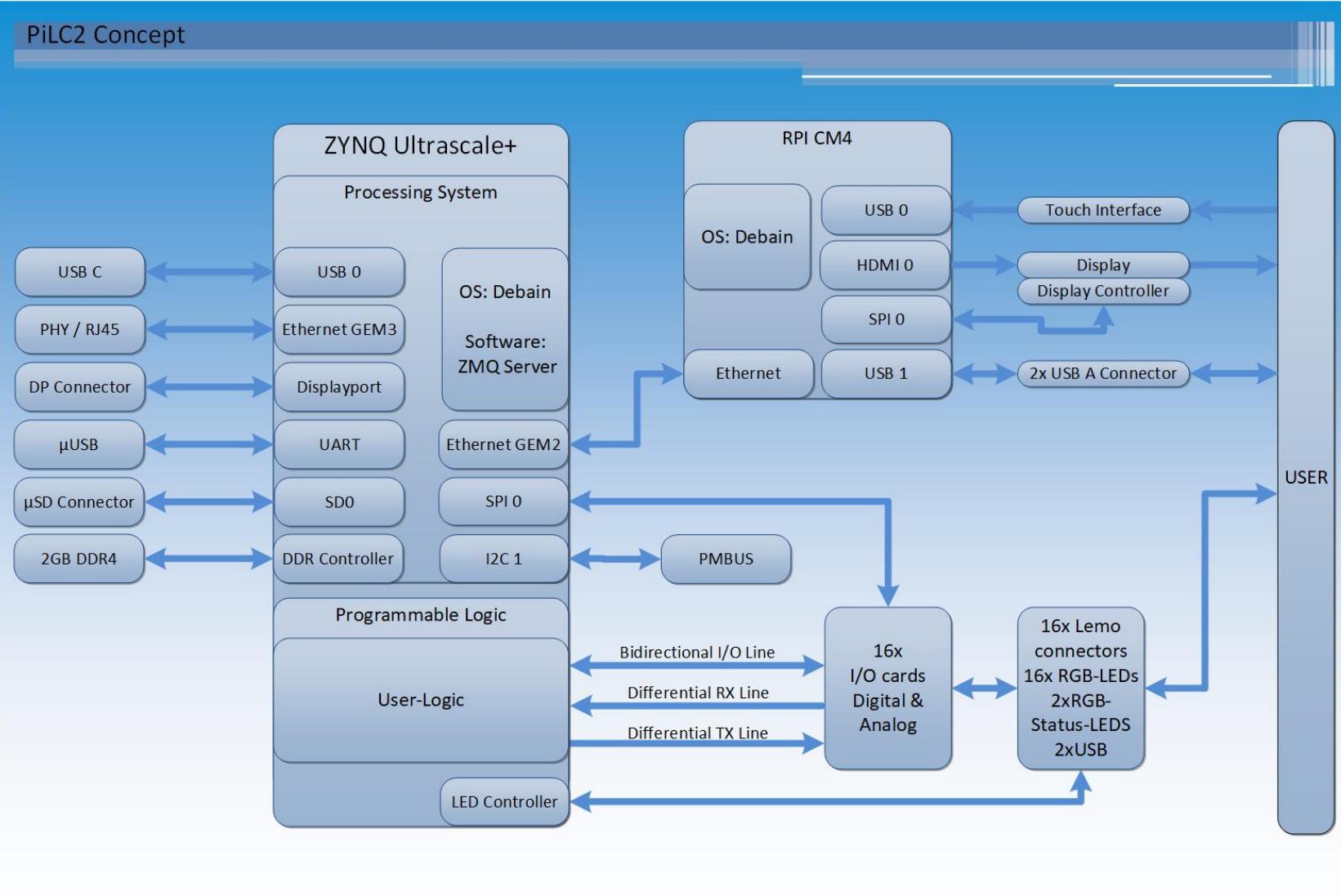
Graph

Out Register 1

Time	Value
10:46:40	7574400
10:46:41	7574395
10:46:42	7574390
10:46:43	7574420
10:46:44	7574400
10:46:45	7574395
10:46:46	7574405
10:46:47	7574410
10:46:48	7574400
10:46:49	7574395
10:46:50	7574405
10:46:51	7574410
10:46:52	7574405
10:46:53	7574410
10:46:54	7574405
10:46:55	7574410
10:46:56	7574405
10:46:57	7574410
10:46:58	7574405

PiLC2 Concept

PiLC2 Concept



- AVNET: UltraZed-EG
 - Xilinx Zynq® UltraScale+™ MPSoC
 - 2GB DDR4
 - Gigabit Ethernet PHY
 - 8GB eMMC Flash
- Raspberry Pi CM4
- Touch Display
 - Size: 4"
 - Resolution 480x800 Pixel
 - Resistive touch display
- RGB-LEDs for I/O status
- Generic ZMQ-Server

PiLC2 Prototyp

- Function blocks in the standard firmware, selectable without new compiling:
 - Direct reading from the I/O Cards:
 - ADC, DADC, Thermo, PT100
 - Up to 14 Gated Counters.
 - Up to 8 Encoder readings.
 - Logic module + Delay function
 - AND, OR, XOR
 - Inverting input/output
 - Delay min.: 50ns
 - Delay steps: 5ns

